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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,038	08/30/2001	Yoshihiro Mori	0819-0637	7302

22204 7590 08/23/2005

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,038	MORI ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 38-60* is/are pending in the application.

4a) Of the above claim(s) *1-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001 and 29 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/30/01, 6/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The examiner thanks the Applicant for resubmitting "Reasons for Rejection," JP 11-11930 and JP 11-07488. All documents submitted on IDS forms dated 8/30/01 and 6/10/03 have been considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 38, 39, 44-48, 52, 55, and 60 are rejected under 35 U.S.C. 102(b) as being anticipated by Patel et al. (U.S. 5,374,578).

Regarding claim 38, Patel et al. teaches a method for fabricating a semiconductor device, the method comprising the steps of: a) forming a metal lower electrode on a substrate (**12** in Fig. 1; column 3, lines 21-28); b) annealing the metal lower electrode in a reducing atmosphere that contains impurity atoms (column 3, lines 29-33—forming gas contains hydrogen, which creates a reducing atmosphere); c) forming a capacitive dielectric film on the metal lower electrode after the step b) (**14** in Fig. 2; column 3, lines 42-62); and d) forming an upper electrode on the capacitive dielectric film (**16** in Fig. 3; column 4, lines 39-44), wherein the impurity atoms are introduced into the metal lower electrode in the step b, which is inherent, as admitted by applicant on page 8, lines 18-20 and page 12, line 16 to page 15, line 2 (see MPEP 2112). Applicants argue on page 4, paragraph 1 of the remarks dated 6/15/05 that these

portions of their specification refer only to their present invention, but this argument is not persuasive because Applicants disclose no special step taken to ensure that the impurity atoms are introduced into the metal lower electrode.

Regarding claim 39, Patel et al. teaches that the impurity atoms are hydrogen atoms (forming gas, column 3, line 32).

Regarding claims 44 and 45, Patel et al. teaches that the capacitive dielectric film is formed in an oxidizing atmosphere in the step c) (column 3, lines 55-59) and further teaches crystallizing the capacitive dielectric film by a heat treatment after the step c) and before the step d) (column 3, line 63 – column 4, line 22).

Regarding claims 46-48, Patel et al. teaches that the metal lower electrode is made of a noble metal, refractory metal (Mo), or Pt (column 3, lines 21-26).

Regarding claims 52 and 55, Patel et al. teaches that the capacitive dielectric film is an insulating film made of an oxide (column 3, lines 54-59) or composed of PZT (column 3, line 52).

Regarding claim 60, Patel et al. teaches that the annealing process is performed at a temperature of 500 °C (column 3, line 32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (U.S. 5,374,578) in view of Schrems et al. (US 2002/0025622 A1).

With respect to claim 40, Patel et al. teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach that the annealing process is performed in an argon atmosphere containing hydrogen.

Schrems et al. teaches a method of fabricating a capacitor comprising the step of annealing the bottom electrode in an argon atmosphere containing hydrogen (paragraphs 0028 and 0035).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method for fabricating a semiconductor device as in Patel et al. and in claim 38 by annealing the lower electrode in an argon atmosphere containing hydrogen, as in Schrems et al. The motivation for doing so at the time of invention would have been to incorporate hydrogen into the lower electrode to enable the use of physically thinner dielectric layers, as expressly taught by Schrems et al. (paragraph 0032).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (U.S. 5,374,578) in view of Dennison et al. (U.S. 5,162,248).

With respect to claim 41, Patel et al. teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach forming an insulating film on the substrate and forming a recess on the insulating film before the step a).

Dennison teaches a method for fabricating a semiconductor device comprising the steps of forming an insulating film on the substrate (**21** in Fig. 2; column 4, lines 45-

47) and forming a recess on the insulating film (**22** in Fig. 2; column 4, lines 60-61, 64-67) before forming a lower electrode on the substrate, wherein the lower electrode is formed in the recess (**51** in Fig. 5; column 4, lines 67-68; column 5, lines 41-43).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of forming a capacitor as taught by Patel et al. and as in claim 38 by forming an insulating film over the substrate and forming a recess on the insulating film before forming the lower electrode on the substrate, wherein the lower electrode is formed in the recess in the step b), as taught by Dennison. The motivation for doing so at the time of invention would have been to provide a support form for the bottom electrode, as expressly taught by Dennison (column 4, lines 64-67).

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (U.S. 5,374,578) in view of Schrems et al. (US 2002/0025622 A1) as applied to claim 40 above, and further in view of Dennison et al. (U.S. 5,162,248).

Together Patel et al. and Schrems et al. teach the method of claim 40 (note 35 U.S.C. 103(a) rejection above), but do not expressly teach the steps of forming an insulating film on the substrate and forming a recess in the insulating film before the step a), wherein the metal lower electrode is formed in the recess in the step b).

Dennison et al. teaches a method for fabricating a semiconductor device comprising the steps of forming an insulating film on the substrate (**21** in Fig. 2; column 4, lines 45-47) and forming a recess on the insulating film (**22** in Fig. 2; column 4, lines 60-61, 64-67) before forming a lower electrode on the substrate, wherein the lower

electrode is formed in the recess (**51** in Fig. 5; column 4, lines 67-68; column 5, lines 41-43).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of forming a capacitor as taught by Patel et al. and Schrems et al. and as in claim 40 by forming an insulating film over the substrate and forming a recess on the insulating film before forming the lower electrode on the substrate, wherein the lower electrode is formed in the recess in the step b), as taught by Dennison. The motivation for doing so at the time of invention would have been to provide a support form for the bottom electrode, as noted above and expressly taught by Dennison (column 4, lines 64-67).

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (U.S. 5,374,578) in view of Kashihara et al. (U.S. 5,382,817).

With respect to claim 43, Patel et al. teaches the method of claim 38, but does not teach that the metal lower electrode has a thickness of 100 nm or less at the thinnest part thereof.

Kashihara et al. teaches a method of forming a capacitor wherein the metal lower electrode has a thickness of 50-100 nm (column 24, claim 3).

Therefore, at the time of the invention, it would have been obvious to modify the method of forming a semiconductor device as taught by Patel et al. and as in claim 38 by making the metal lower electrode with a thickness of 100 nm or less at the thinnest part thereof, as taught by Kashihara et al. The motivation for doing so at the time of invention would have been to provide a semiconductor device with sufficient capacity for

memory storage as the device is miniaturized, as taught by Kashihara et al. (column 6, lines 45-48).

Claims 49-51, 53, 56, 57, and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (U.S. 5,374,578) in view of Park et al. (U.S. 6,180,447).

With respect to claims 49-51, Patel et al. teaches the method of claim 38, but does not expressly teach that the lower electrode is composed of Ir, Ru, or Rh.

Park et al. teaches a method for fabricating a capacitor wherein the metal lower electrode is composed of Ir, Ru, or Rh (column 1, lines 45-46).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of forming a semiconductor device as taught by Patel et al. and as in claim 38 by forming the lower electrode of Ir, Ru, or Rh, as taught by Park et al. The motivation for doing so at the time of invention would have been because these metals have excellent oxidation resistance, as expressly taught by Park et al. (column 1, lines 47-48).

Regarding claims 53, 56, 57, and 59, Patel et al. teaches the method of claim 38, but does not teach that the capacitive dielectric film is composed of BST or Ta_2O_5, or that the metal lower electrode is composed of Ru and the capacitive dielectric film is composed of Ta_2O_5 or that the metal lower electrode is composed of Ir and the capacitive dielectric film is composed of PZT.

Park et al. teaches a method for fabricating a capacitor wherein the capacitive dielectric film is composed of BST or Ta_2O_5, the metal lower electrode is composed of Ru and the capacitive dielectric film is composed of Ta_2O_5, and wherein the metal lower

electrode is composed of Ir and the capacitive dielectric film is composed of PZT (column 1, lines 35-54).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Patel et al. and Park et al. to manufacture a capacitor according to the method taught by Patel et al. and by claim 38, wherein the capacitive dielectric film is composed of BST or Ta_2O_5, the metal lower electrode is composed of Ru and the capacitive dielectric film is composed of Ta_2O_5, or the metal lower electrode is composed of Ir and the capacitive dielectric film is composed of PZT, as taught by Park et al. The motivation for doing so at the time of the invention would have been because these metals have excellent oxidation resistance (column 1, lines 47-48) and the dielectrics lead to increased capacitance (column 1, lines 35-39), as expressly taught by Park et al.

Claims 54 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (U.S. 5,374,578) in view of Nagata et al. (U.S. 2002/0011615).

Regarding claims 54 and 58, Patel et al. teaches the method of claim 38, but does not teach that the capacitive dielectric film is composed of SBT or that the metal lower electrode is composed of Ir and the capacitive dielectric film is composed of SBT.

Nagata et al. teaches a method of forming a capacitor wherein the capacitive dielectric film is composed of SBT (paragraph 0056) and the metal lower electrode is composed of Ir (paragraph 0046).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate a capacitor using the method taught by Patel et al.

and by claim 38 and further form the capacitive dielectric film of SBT and the metal lower electrode of Ir. The motivation for doing so would have been that Ir has excellent barrier properties (paragraph 0012) and SBT is a commonplace oxide ferroelectric material used as a dielectric film over a bottom electrode (paragraph 0056), as expressly taught by Nagata et al., and using such a material would avoid the cost and time of exploring or developing new materials.

Response to Arguments

Applicant's arguments with respect to claims 38-60 (see pages 3-4 of the remarks filed 6/15/05) have been fully considered. The examiner does not agree that ruthenium oxide is an insulating oxide, as asserted on page 3 of Applicant's remarks, since Takeshi (JP 11-150245) discloses in paragraph 2 that it is a conductive oxide. However, Applicant's argument that Takeshi discloses annealing ruthenium oxide, a conductive oxide of a metal, but not a metal itself, in a reducing atmosphere that contains impurity atoms, is persuasive, but moot in view of the new grounds of rejection.

Additionally, as indicated above, Applicants argue on page 4, paragraph 1 of the remarks that these portions of their specification refer only to their present invention, but this argument is not persuasive because Applicants disclose no special step taken to ensure that the impurity atoms are introduced into the metal lower electrode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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